



# 點通科技股份有限公司

## SPECIFICATION

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PRODUCT NAME : PT7686W-S\*\*

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

# PTCOM Technology

## PT7686W-S

PT7686W-SA: Wi-Fi 802.11b/g/n+MCU+Chip Antenna

PT7686W-SC: Wi-Fi 802.11b/g/n+MCU+RF connector

PT7686W-SP: Wi-Fi 802.11b/g/n+MCU+RF pinout

### Product Specification Sheet

#### Revision History

Date	Revision Content	Revised By	Version
2017/06/21	-Preliminary Specification	Howard.Chen	0.1
2017/12/01	Spec revision	Howard.Chen	0.2
2018/08/23	Power Consumption updated	Howard.Chen	0.5
2018/08/24	Memory Flash updated	Howard.Chen	0.6

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# 1. Introduction

PT7686W-S\*\* series are a low-cost, low-power consumption and highly-integrated embedded 1X1 11b/g/n single-band Wi-Fi module specially designed for IOT (Internet of Things) market. This module adopts the SOC chip from MTK which contains an ARM Cortex-M4F MCU application process running at 192MHz, Wi-Fi subsystem and power management unit (PMU).

PT7686W-S\*\* series have embedded 384KB SRAM, 32KB L1 cache, 4MBs pseudo SRAM with half sleep mode current: 10 $\mu$ A and 4MB serial flash, running at RTOS environment. It also support many peripherals which including SPI, SDIO, I2S, I2C, UART, PWM and auxiliary ADC. This is perfectly suitable for all variety of applications in the IOT market.

A dedicated high-performance 32-bit RISC CPU N9 up to 160MHz clock speed is implemented to achieve robust Wi-Fi connection with support variety of security encryptions. PT7686W-S\*\* series compliant with IEEE 802.11 b/g/n standard with 20MHz and 40MHz bandwidth and up to 150Mbps data rate.

Highly integrated PT7686W-S\*\* series modules enable easy configurations, all types of power saving mode to maximize battery life, seamless roaming capabilities and advanced security. It can be also interact with different access point (AP) from different vendors.

A high-performance printed antenna is designed on the module to obtain low-cost, easy to use and compact module size. PT7686W-S\*\* series modules also provide several RF connector variants (ex. PT7686W-SC\*, PT7686-SA\*, PT7686-SP\*) that allow customers to use external antenna when it is required.

## 2. Features

### 2.1. System and WiFi

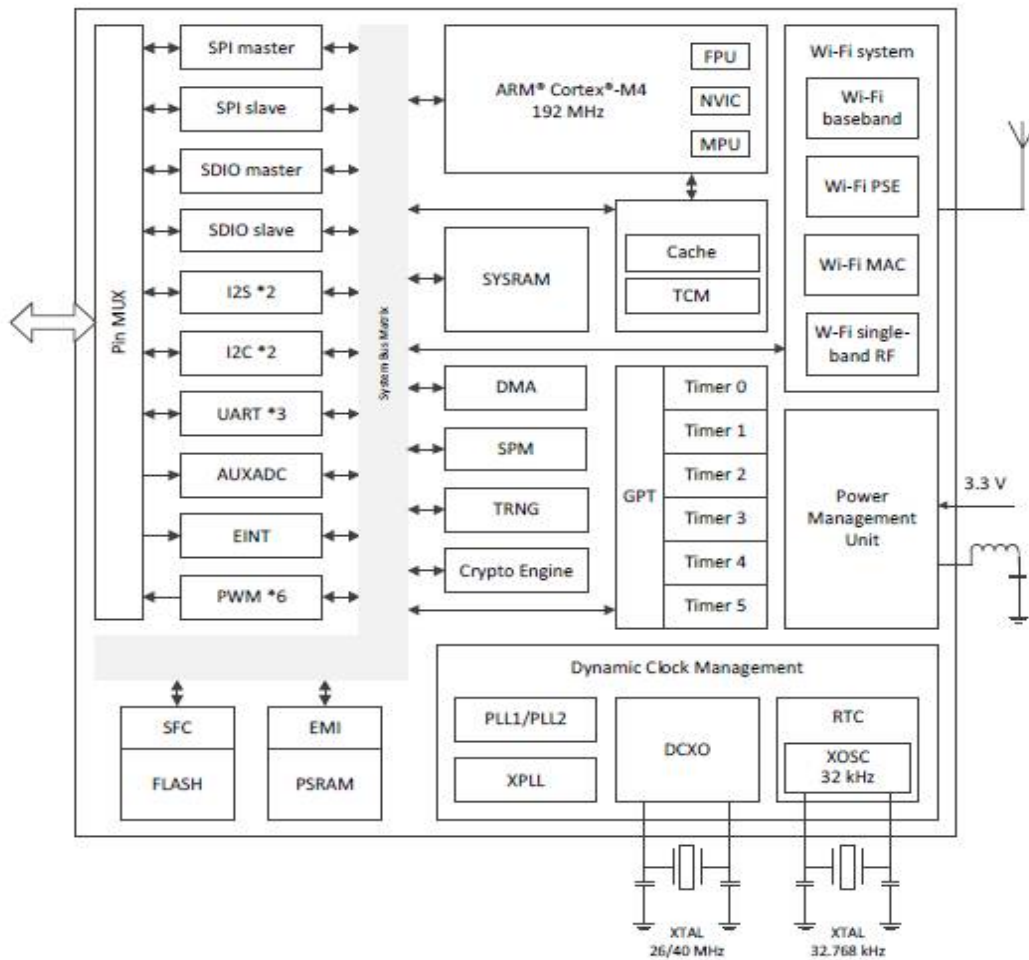
- Integrated ARM Cortex-M4F MCU with on-chip memory enables running IEEE802.11 firmware that can be field-upgraded with future features.
- 384KB SRAM, 32KB L1 cache, with high hit rate, zero-wait state, maximum frequency at 192MHz
- Embedded 32Mbits flash, with less than 0.1μA
- Embedded 32Mbits pseudo SRAM with half sleep mode current: 10μA
- Supports 20MHz, 40MHz bandwidth in 2.4GHz band
- Wi-Fi security
  - WEP/WPA2/WPS
  - WPA2-Enterprise
- Wi-Fi direct, SoftAP, sniffer
- Dynamically switching between STA and SoftAP modes at runtime
- MediaTek Smart Connection
- RX antenna diversity
- Crypto engine
  - AES 128, 192, 256 bits
  - DES, 3DES
  - MD5, SHA-1, 224, 256, 384, 512

### 2.2. Interface

- One SPI master interface, 1, 2 or 4-bit mode, up to 48MHz
- One SPI slave interface, 1, 2 or 4-bit mode, up to 48MHz
- One SDIO host interface (v2.0)
- One SDIO device interface (v2.0)
- One I2S interface supporting 16 or 24-bit, master or slave mode (supports 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz sample rates, transmit or receive, two channels)
- One I2S interface supporting 16-bit, master or slave mode (supports TDM mode) (supports 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz sample rates, transmit or receive, two channels)
- Up to three UART interfaces with hardware flow control (~3Mbps)
- Up to two I2C master interfaces (3.4Mbps)
- Up to four channels of 12-bit ADC
- Up to six PWM channels
- Up to 21 GPIO interfaces with 5V-tolerant fast IOs, each IO can be configured as an external interrupt source



A simplified block diagram of the module is depicted in the figure below.



### 3. General Specification

#### 3.1 General Specification

Model Name	PT7686W-S**
Product Description	Wi-Fi 802.11b/g/n + MCU Module
PCBA Dimension	21 mm x 15 mm x 2.2mm +/-0.5mm
PCB Dimension	21 mm x 15 mm x 0.6mm +/-0.1mm
Module Interface	SPI, SDIO, I2S, I2C, UART, PWM, ADC.
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95%

## 3.2 Voltages

### 3.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VDD_3V3	Power supply for SIP Module	-0.3	3.63	V

### 3.2.2 Recommended Operating Ratings

Symbol	Min.	Typ.	Max.	Unit
VDD_3V3	3.0	3.3	3.6	V
RTC_3V3	1.7		3.6	

### 3.2.2 DC Characteristics

Symbol	Parameter	Conditions	Min	Max.	Unit
V <sub>IL</sub>	Input Low Voltage	LVTTL	-0.28	0.8	V
V <sub>IH</sub>	Input High Voltage	LVTTL	2	3.6	V
V <sub>OL</sub>	Output Low Voltage	I <sub>oL</sub>   = 4~16mA	-0.28	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>oH</sub>   = 4~16mA	2.4	3.6	V
R <sub>PU</sub>	Input Pull-UP Resistance	PU=high, PD=low	40	190	KΩ
R <sub>PD</sub>	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ



## 4. Wi-Fi RF Specification

### 4.1 2.4GHz RF Specification

Conditions : VDD\_3V3=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz : Ch1 ~ Ch14
Modulation	802.11b : CCK, DQPSK, DBPSK 802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK
TX Output Power	802.11b /11Mbps : 18 dBm , typical @ EVM ≤ -9dB
	802.11g / 6Mbps : 18 dBm , typical @ EVM ≤ -5dB
	802.11g /54Mbps : 16 dBm , typical @ EVM ≤ -25dB
	HT20/11n /MCS0 : 18 dBm , typical @ EVM ≤ -5dB
	HT20/11n /MCS7 : 16 dBm , typical @ EVM ≤ -28dB
	HT40/11n /MCS0 : 15 dBm , typical @ EVM ≤ -5dB
	HT40/11n /MCS7 : 15 dBm , typical @ EVM ≤ -27dB
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -93dBm, typical
	- 2Mbps PER @ -90Bm, typical
	- 5.5Mbps PER @ -89 dBm, typical
	- 11Mbps PER @ -86 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -91Bm, typical
	- 9Mbps PER @ -88dBm, typical
	- 12Mbps PER @ -88dBm, typical
	- 18Mbps PER @ -85dBm, typical
	- 24Mbps PER @ -82dBm, typical
	- 36Mbps PER @ -78Bm, typical
	- 48Mbps PER @ -74dBm, typical
	- 54Mbps PER @ -72dBm, typical
Receive Sensitivity (11n,20MHz, 800ns) @10% PER	- MCS=0 PER @ -88dBm, typical
	- MCS=1 PER @ -86dBm, typical
	- MCS=2 PER @ -84dBm, typical
	- MCS=3 PER @ -81dBm, typical
	- MCS=4 PER @ -78Bm, typical
	- MCS=5 PER @ -74 dBm, typical
	- MCS=6 PER @ -72 dBm, typical

	- MCS=7 PER @ -70 dBm, typical
Receive Sensitivity (11n,40MHz, 800ns) @10% PER	- MCS=0 PER @ -88.5dBm, typical
	- MCS=1 PER @ -81dBm, typical
	- MCS=2 PER @ -80dBm, typical
	- MCS=3 PER @ -76dBm, typical
	- MCS=4 PER @ -73dBm, typical
	- MCS=5 PER @ -70 dBm, typical
	- MCS=6 PER @ -67 dBm, typical
	- MCS=7 PER @ -66 dBm, typical
Channel Rejection	- 11Mbps 40dBm, typical
	- 6Mbps 34dBm, typical
	- 54Mbps 22dBm, typical
	- HT20 MCS=0 33dBm, typical
	- HT20 MCS=7 15dBm, typical
	- HT40 MCS=0 29dBm, typical
	- HT40 MCS=7 9dBm, typical
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
(20MHz ,Long GI,800ns)	802.11n : 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
(20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Reference	On board Antenna: PT7686W-SA* Small antennas with 0 dBi peak gain U.FL connector for external antenna: PT7686W-SC* RF output pin for external antenna: PT7686W-SP*

## 4.2 Power Consumption

Conditions: VDD\_3V3=3.3V ; Temp:25°C (TBD)

Mode	Description	Typ.	Unit
Retention	<ul style="list-style-type: none"> <li>● RTC Timer</li> <li>● 0KB SRAM data retention</li> </ul>	2.7	uA
	<ul style="list-style-type: none"> <li>● RTC Timer</li> <li>● 8KB SRAM data retention</li> </ul>	4.7	uA
Sleep	<ul style="list-style-type: none"> <li>● Cortex-M4 in sleep state</li> <li>● TCM 96KB SRAM is retained</li> <li>● SYSRAM 384KB SRAM is retained</li> <li>● XTAL 32kHz</li> </ul>	120	uA
Active Mode TX Power	<ul style="list-style-type: none"> <li>● CCK 19 dBm</li> <li>● N9 in Idle State</li> <li>● Cotext-M4 in sleep state</li> <li>● TCM 96KB SRAM is retained</li> <li>● XTAL 32K Hz</li> </ul>	248	mA
	<ul style="list-style-type: none"> <li>● OFDM 16.5 dBm</li> <li>● N9 in Idle State</li> <li>● Cotext-M4 in active state</li> <li>● TCM 96KB SRAM is retained</li> <li>● XTAL 32K Hz</li> </ul>	220	mA
Active Mode RX Power	<ul style="list-style-type: none"> <li>● HT20_MCS7</li> <li>● N9 in Idle State</li> <li>● Cotext-M4 in active state</li> <li>● XTAL 32K Hz</li> </ul>	42	mA
	<ul style="list-style-type: none"> <li>● HT20_MCS7</li> <li>● N9 in Idle State</li> <li>● Cotext-M4 in sleep state</li> <li>● XTAL 32K Hz</li> </ul>	30	mA
Active & Sleep DTIM=1	<ul style="list-style-type: none"> <li>● Cotext-M4 in sleep state</li> <li>● TCM 96KB SRAM is retained</li> <li>● XTAL 32K</li> </ul>	630	uA

## 5. Peripheral interface

Several peripheral interfaces are multiplexed with GPIOs. PT7686W-S\* has three dedicated UART interfaces with flow control, two dedicated I2C interface, and one dedicated IrDA interface, one Master SPI and one Slave SPI interface, one Master SDIO, one Slave SDIO ,and two I2S interfaces.

### 5.1 GPIOs

Each of the General Purpose Input/Output (GPIO) pins are software configurable as an output (push-pull or open-drain) or as an input (with or without pull-up or pull-down) that supports input floating with buffer gating to reduce power consumption. Most of the GPIOs are multiplexed with peripheral functions and have selectable output driving strength.

### 5.2 UART interface

There are 3 UART interfaces that provide full duplex serial communication between the baseband chipset and external devices. UART has both M16C450 and M16550A modes of operation compatible with a range of standard software drivers.

UARTs support baud rates from 110bps up to 921,600bps and baud rate auto-detection function. They provide hardware and software flow control of the RTS/CTS signals.

UARTs can configure data transfer lengths from 5 to 8 bits, with an optional parity bit and one or two stop bits by software. They can be served by the DMA controller..

### 5.3 I2C Serial Interface

There are two I2C master controllers and three types of speed modes in the I2C controllers: standard mode (100kbit/s), fast mode (400kbit/s) and high-speed mode (3.4Mbit/s), supporting 7-bit/10-bit addressing and can be served by the DMA controller. The I2C package size supports up to 1,024 bytes per transfer and 1,024 transfers per transaction in DMA mode and 8 bytes per transfer in non-DMA mode. START/STOP/REPEATED START condition can be increased to support single or multi transfer. These features can be configured by software based on customers' requirements.

### 5.4 Auxiliary ADC function

PT7686W-S\* features 4 auxiliary ADC channels. The sample rate is 0.5 MSPS, DNL accuracy is 1LSB.

## 5.5 SPI Master Interface

There are one SPI master controller and one SPI slave controller to receive and transmit device data using single, dual and quad SPI protocol. The SPI controllers can communicate at up to 48 Mbps.

The chip select signal and SPI clock of SPI master controllers are configurable. The SPI controllers also support DMA mode for large amounts of data transmission.

## 5.6 I2S interface

PT7686W-S\* provides Inter-IC Sound Interface (I2S) controllers. The controllers can be selected as master or slave. There are two types of transfer protocols in the I2S controllers: one is the I2S protocol, supporting 24-bit/16-bit addressing and mono/stereo transaction; the other one is the TDM protocol, supporting 16-bit addressing and TDM32/TDM64/TDM128 transaction. I2S controllers can be served by the DMA controller and the sample rate can support either 16/24/48/96/192kHz or 11.025/22.05/44.1kHz when sharing only one internal PLL. Detailed specifications of the I2S and TDM are shown in Table 2.5-1 and Table 2.5-2.

*Table 2.5-1. I2S protocol specifications*

I2S Protocol	Bit Width	Input/output Sample
Master Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, mono/stereo
	I2S1: 16b/24b	XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo
Slave Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, mono/stereo
	I2S1: 16b/24b	XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo

*Table 2.5-2. TDM protocol specifications*

TDM Protocol	Bit Width	Input/output Sample
Master Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, TDM32/TDM64 XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, TDM32/TDM64 XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, TDM32/TDM64
Slave Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128) XPLL 22.5792MHz (either of the following): <ul style="list-style-type: none"> <li>• 11.025, 22.05, 44.1, 88.2 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128)</li> <li>• 176.4 kHz, TDM32/TDM64</li> </ul> XPLL 24.576MHz (either of the following): <ul style="list-style-type: none"> <li>• 8, 12, 16, 24, 32, 48, 96 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128)</li> <li>• 192 kHz, TDM32/TDM64</li> </ul>

## 5.7 Pulse Width Modulation (PWM)

There are six PWM controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals can be programmed. The PWM controllers can be configured to use 40MHz, 13MHz or 32kHz clock source to support a wide range of output pulse frequencies..

## 5.8 SD memory card controller

PT7686W-SX supports SD memory card bus protocol, as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0.

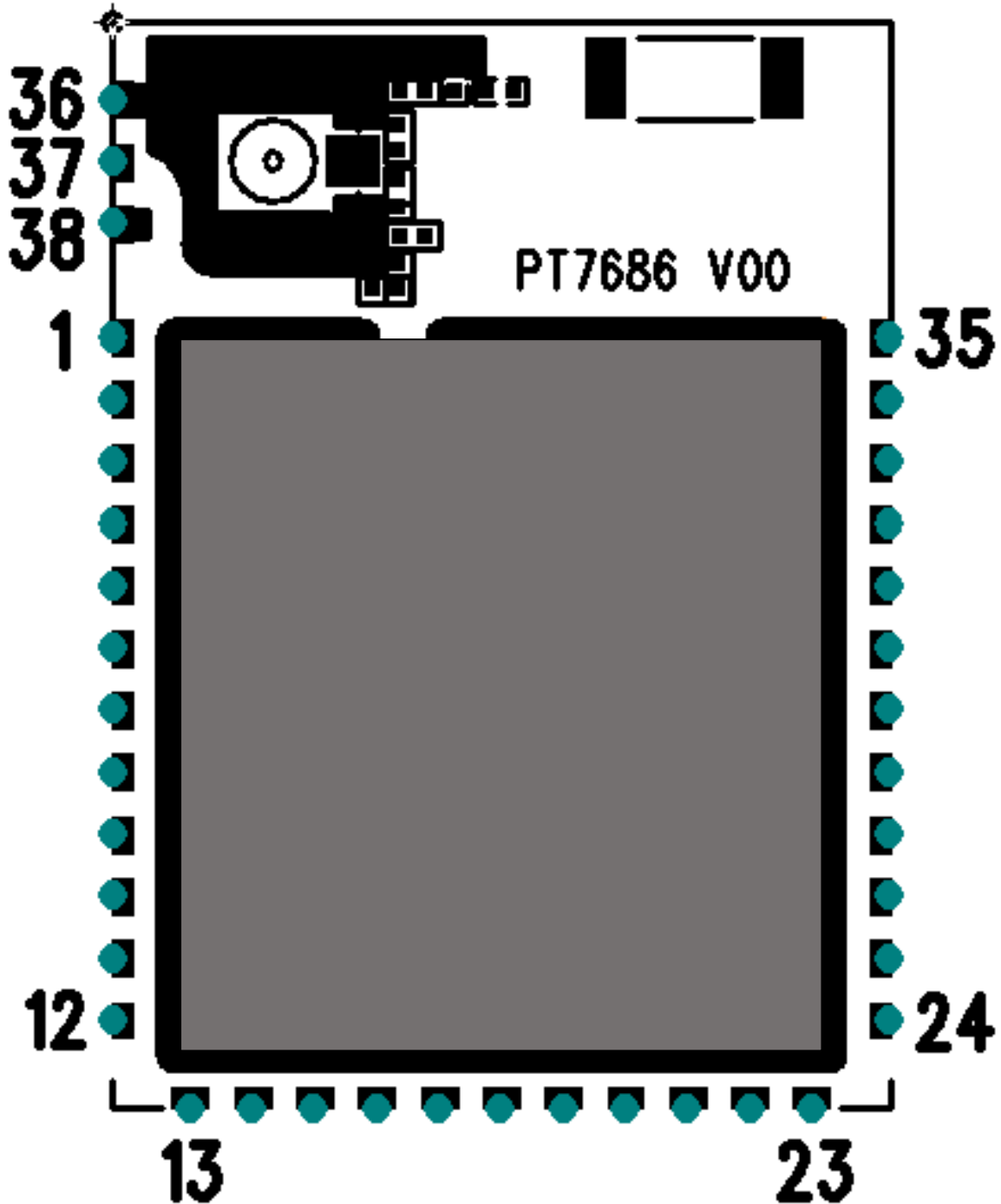
Furthermore, the controller also partially supports the SDIO card specification version 2.0. However, the controller can only be configured as the host of the SD memory card.

Main features of the controller:

- 32-bit access for control registers
- 8, 16, or 32-bit access for FIFO in PIO mode
- Built-in CRC circuit
- Supports PIO mode, basic DMA mode and descriptor DMA mode for SD controller.
- Interrupt capabilities
- Data rate of up to 48Mbps in 1-bit mode, 48x4 Mbps in 4-bit mode. The module is targeted at 48MHz operating clock
- Programmable serial clock rate on SD bus (256 gears)
- Card detection capabilities (MT7686 uses the EINT controller for card detection )
- Does not support SPI mode for SD memory card
- Does not support suspend/resume for SD memory card.

## 6. Pin Assignments

### 6.1 PT7686/7686W-S PCB Pin Outline (TOP view)



## 6.2 Pin Description

Each pin is multiplexed with several functions, the default setting is colored in below table.

No	Name	Pin Type	Power Domain	Description
1	GPIO20	I/O	DVDD_IO_0	General purpose input, output
	UTXD0	O		UART(0) TXD
	EINT20	I		External interrupt
	AUXADC3	I		Auxiliary ADC input
2	GPIO19	I/O	DVDD_IO_0	General purpose input, output
	URXD0	I		UART(0) RXD
	EINT19	I		Auxiliary ADC input
	SCL1	I/O		I2C(1) SCL
	PWM5	O		Pulse-width-modulated output
	AUXADC2	I		Auxiliary ADC input
	WIFI_EXT_CLK	I		External 32kHz clock
3	GPIO 18	I/O	DVDD_IO_0	General purpose input, output
	PMU_GOTO_SLEEP			
	TDM_MCLK			TDM Master Clock
	CLKO4	O		CLK4 OUT
	SDA1	I/O		I2C(1) SDA
	AUXADC1	I		Auxiliary ADC input
	EINT18	I		External interrupt
	CLKO3	O		CLK3 OUT
	PMU_RGU_RSTB			
4	GPIO17	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_B_CS	O		SPI CS
	SPIMST_B_CS	O		SPI CS
	TDM_CK	O		TDM CLK
	PWM5	O		Pulse-width-modulated output
	CLKO3	O		CLK3 OUT
	AUXADC0	I		Auxiliary ADC input
	EINT17	I		External interrupt
	BT_PRI0	O		BT Priority(0)
5	GND	-	-	-
6	GPIO16	I/O	DVDD_IO_0	General purpose input, output



	SPISLV_B_SCK	O		SPI CLK
	SPIMST_B_SCK	O		SPI CLK
	TDM_WS	I/O		I2S WS
	MA_MC0_DA3	I/O		SDIO Master Data3
	SLV_MC0_DA3	I/O		SDIO Slave Data3
	SDA1	I/O		I2C(1) SDA
	EINT16	I		External interrupt
.7	GPIO15	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_B_SIO0	O		SPI MOSI
	SPIMST_B_SIO0	O		SPI MOSI
	TDM_TX	O		I2S TX
	MA_MC0_DA2	I/O		SDIO Master Data2
	SLV_MC0_DA2	I/O		SDIO Slave Data2
	SCL1	I/O		I2C(1) SCL
	EINT15	I		External interrupt
	PWM3	O		Pulse-width-modulated output
8	GND	-	-	-
9	GPIO14	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_B_SIO1	I		SPI MISO
	SPIMST_B_SIO1	I		SPI MISO
	TDM_RX	I		I2S RX
	MA_MC0_DA1	I/O		SDIO Master Data1
	SLV_MC0_DA1	I/O		SDIO Slave Data1
	PWM4	O		Pulse-width-modulated output
	EINT14	I		External interrupt
	CLKO4	O		CLK4 OUT
10	GPIO13	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_B_SIO2	O		SPI WP
	SPIMST_B_SIO2	O		SPI WP
	U2RTS	O		UART(2) RTS
	MA_MC0_DA0	I/O		SDIO Master Data0
	SLV_MC0_DA0	I/O		SDIO Slave Data0
	CLKO4	O		CLK4 OUT
	EINT13	I		External interrupt
	I2S_WS	I/O		I2S WS
11	GPIO12	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_B_SIO3	O		Slave SPI Data3

	SPI MST_B_SIO3	O		Mast SPI Data3
	UTXD2	O		UART(2) TXD
	MA_MC0_CM0	O		SDIO Master CMD
	SLV_MC0_CM0	O		SDIO Slave CMD
	EINT12	I		External interrupt
	WiFi_ANT_SEL1	O		WiFi ANT Select(1)
	I2S_TX	O		I2S TX
12	GPIO11	I/O	DVDD_IO_0	General purpose input, output
	EINT11	I		External interrupt
	PWM3	O		Pulse-width-modulated output
	URXD2	I		UART(2) RXD
	MA_MC0_CK	O		SDIO Master CLK
	SLV_MC0_CK	O		SDIO Slave CLK
	CLKO2	O		CLK2 OUT
	WiFi_ANT_SEL0	O		WiFi ANT Select(0)
	I2S_RX	I		I2S RX
13	GND	-	-	-
14	RTC_EINT	I/O	AVDD33_VRTC	Dedicate EINT input in RTC
15	EXT_PWR_EN	O	AVDD33_VRTC	PMU enable
16	VRTC	P	-	RTC domain power supply
17	CHIP_EN	I	AVDD33_VRTC	Chip enable
18	DVDD_IO_0	P		Power input of GPIO right group (VIO_0)
19	VDD	P		3.3V
20	DVDD_IO_1	P		Power input of GPIO left group (VIO_1)
21	DVDD18	P		1.8V
22	V2P5NA	P		
23	GPIO10	I/O	DVDD_IO_0	General purpose input, output
	ENIT10	I		External interrupt
	U2CTS			UART(2) CTS
	PWM2	O		Pulse-width-modulated output
	PMU_RGU_RSTB			
	PMU_GOTO_SLEEP			
	WiFi_ANT_SEL4			WiFi ANT Select(4)
	SDA0			I2C(0) SDA
24	GPIO9	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_A_SIO1	I/O		Slave SPI Data1
	SPI MST_A_SIO1	I/O		Master SPI Data1

	EINT9	I		External interrupt
	SDA0	I/O		I2C(0) SDA
	U0CTS			UART(0) CTS
	TDM_MCLK	O		TDM Master CLK
	WiFi_ANT_SEL3	O		WiFi ANT Select(3)
	BT_PRI1	O		BT Priority(1)
25	GND	-	-	-
26	GPIO7	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_A_SCK	I		Slave SPI SCK
	SPIMST_A_SCK	O		Master SPI SCK
	EINT7	I		External interrupt
	CLK01	O		CLK1 OUT
	WIFI_ANT_SEL2	O		WiFi ANT Select(2)
	TDM_WS			TDM WS
	BT_PRI3			BT Priority(3)
27	GPIO8	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_A_SIO0	I/O		Slave SPI Data0
	SPIMST_A_SIO0	I/O		Slave SPI Data0
	EINT8	I		External interrupt
	SCL0	O		I2C(0) SCL
	U0RTS	O		UART(0) RTS
	TDM_CK	O		TDM CLK
	BT_PRI1	O		BT Priority(1)
28	GPIO6	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_A_CS	I		Slave SPI CS
	SPIMST_A_CS	O		Master SPI CS
	EINT6	I		External interrupt
	UTXD0	O		UART(0) TXD
	WiFi_ANT_SEL1	O		WiFi ANT Select(1)
	TDM_TX	O		TDM TX
	SDA0	I/O		I2C(0) SDA
29	GPIO5	I/O	DVDD_IO_0	General purpose input, output
	SPISLV_A_SIO3	I/O		Slave SPI Data3
	SPIMST_A_SIO3	I/O		Master SPI Data3
	EINT5	I		External interrupt
	URXD0	I		UART(0) RXD
	WiFi_ANT_SEL0	O		WiFi ANT Select(0)

	TDM_RX	I		TDM RX
	SCL0	O		I2C(0) CLK
	PMU_RGU_RT SB			
30	GND	-	-	-
31	GPIO4	I/O	DVDD_IO_1	General purpose input, output
	SPI SLV_A_SIO2	O		Slave SPI Data2
	SPI MST_A_SIO2	O		SPI WP
	EINT4	I		External interrupt
	I2S_MCLK	O		I2S MCLK
	JTDO	O		JTAG TDO
	WiFi_ANT_SEL3	O		WiFi ANT Select(3)
	I2S_MCLK	O		I2S MCLK
32	GPIO2	I/O	DVDD_IO_1	General purpose input, output
	EINT2	I		External interrupt
	URXD1	I		UART(1) RXD
	PWM0	O		Pulse-width-modulated output
	I2S_WS	I/O		I2S WS
	JTCK	I		JTAG CLK
	CLKO0	O		CLK0 OUT
	BT_PRI0	O		BT Priority(0)
	WiFi_ANT_S EL4	O		WiFi ANT Select(4)
33	GPIO3	I/O	DVDD_IO_1	General purpose input, output
	EINT3	I		External interrupt
	UTXD1	O		UART(1) TXD
	PWM1	O		Pulse-width-modulated output
	I2S_CK	O		I2S CLK
	JTRST_B	I		JTAG RST_B
	WiFi_ANT_S EL2	O		WiFi ANT Select(2)
34	GPIO1	I/O	DVDD_IO_1	General purpose input, output
	EINT1	I		External interrupt
	U1CTS	I		UART(1) CTS
	SDA1	I/O		I2C(1) SDA
	I2S_TX	O		I2S TX
	JTMS	I		JTAG TMS
	WiFi_ANT_S EL1	O		WiFi ANT Select(1)
	BT_PRI3	O		BT Priority(3)
	PWM1	O		Pulse-width-modulated output

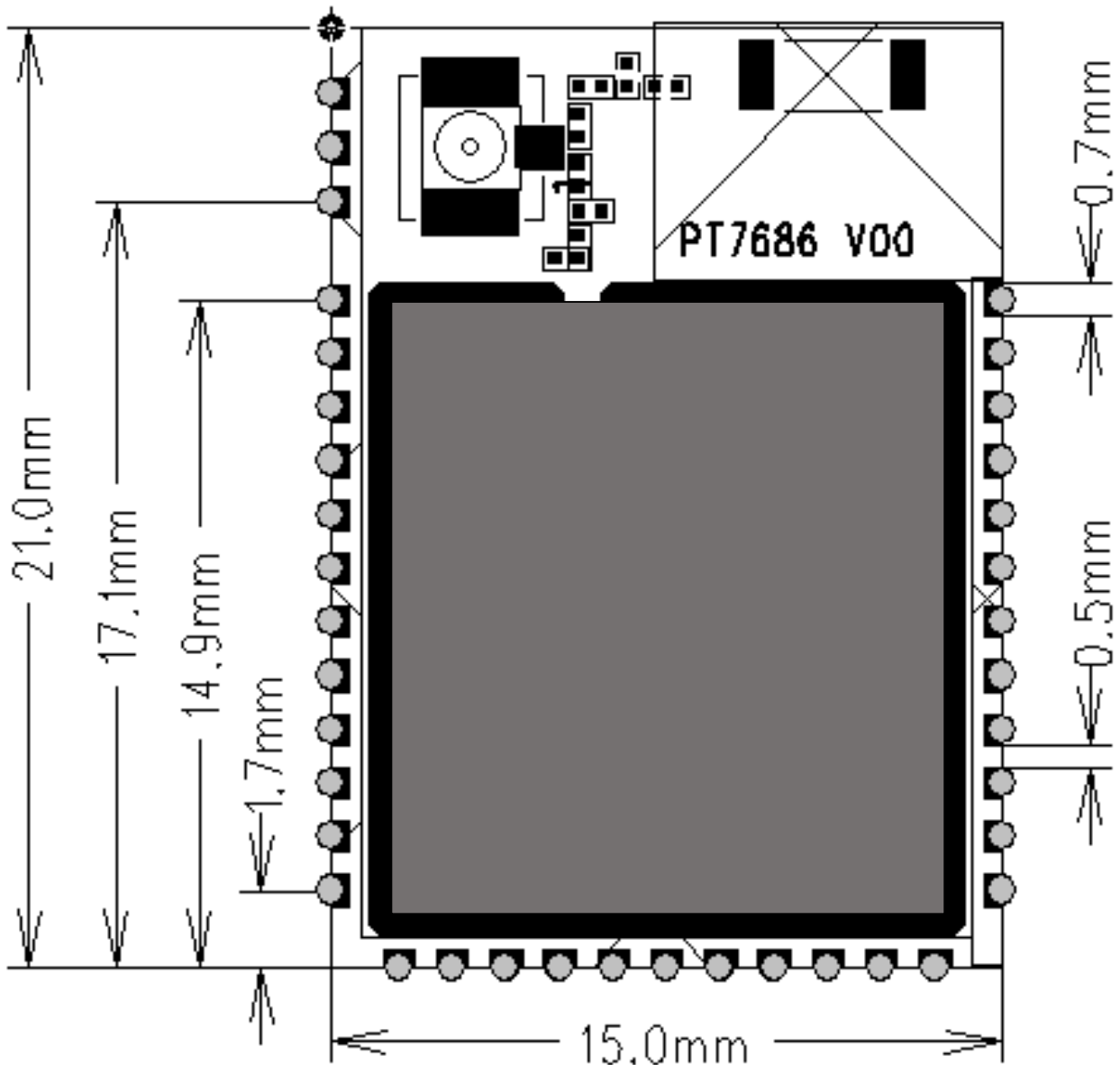
35	GPIO0	I/O	DVDD_IO_1	General purpose input, output
	EINT0	I		External interrupt
	U1RTS	O		UART(1) RTS
	SCL1	I/O		I2C(1) SCL
	I2S_RX	I		I2S RX
	JTDI	I		JTAG TDI
	WIFI_ANT_S EL0	O		WiFi ANT Select(0)
	BT_PRI1	O		BT Priority(1)
	PWM0	O		Pulse-width-modulated output
36	GND	-	-	-
37	RF_PAD			RF Port
38	GND	-	-	-

# 7. Dimensions

## 7.1 PT7686/7686W-S Physical Dimensions

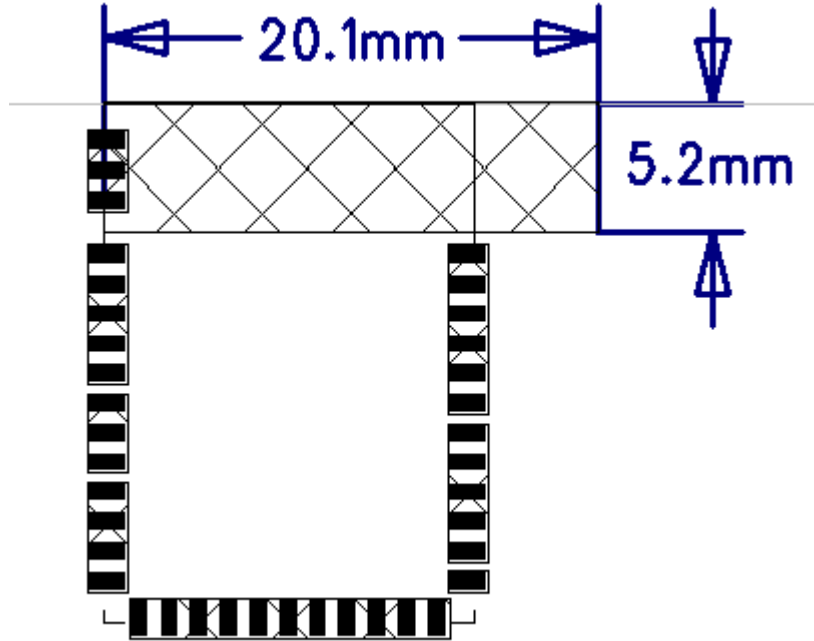
(TOP view)

Note: Pin pitch = 1.2mm, pad width = 0.7mm

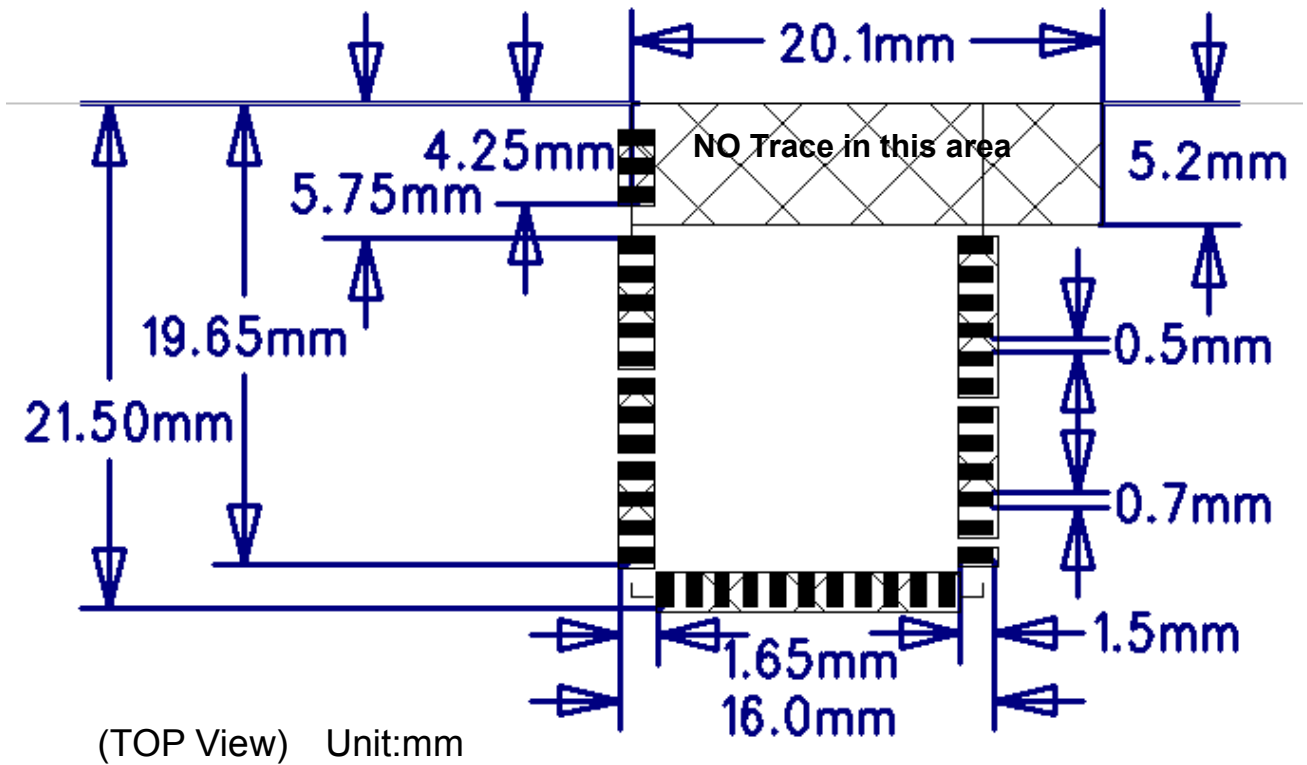


## 7.2 Layout Recommendation

Note: Please place the module at the edge of the board and the antenna keep out area at the PCB edge.



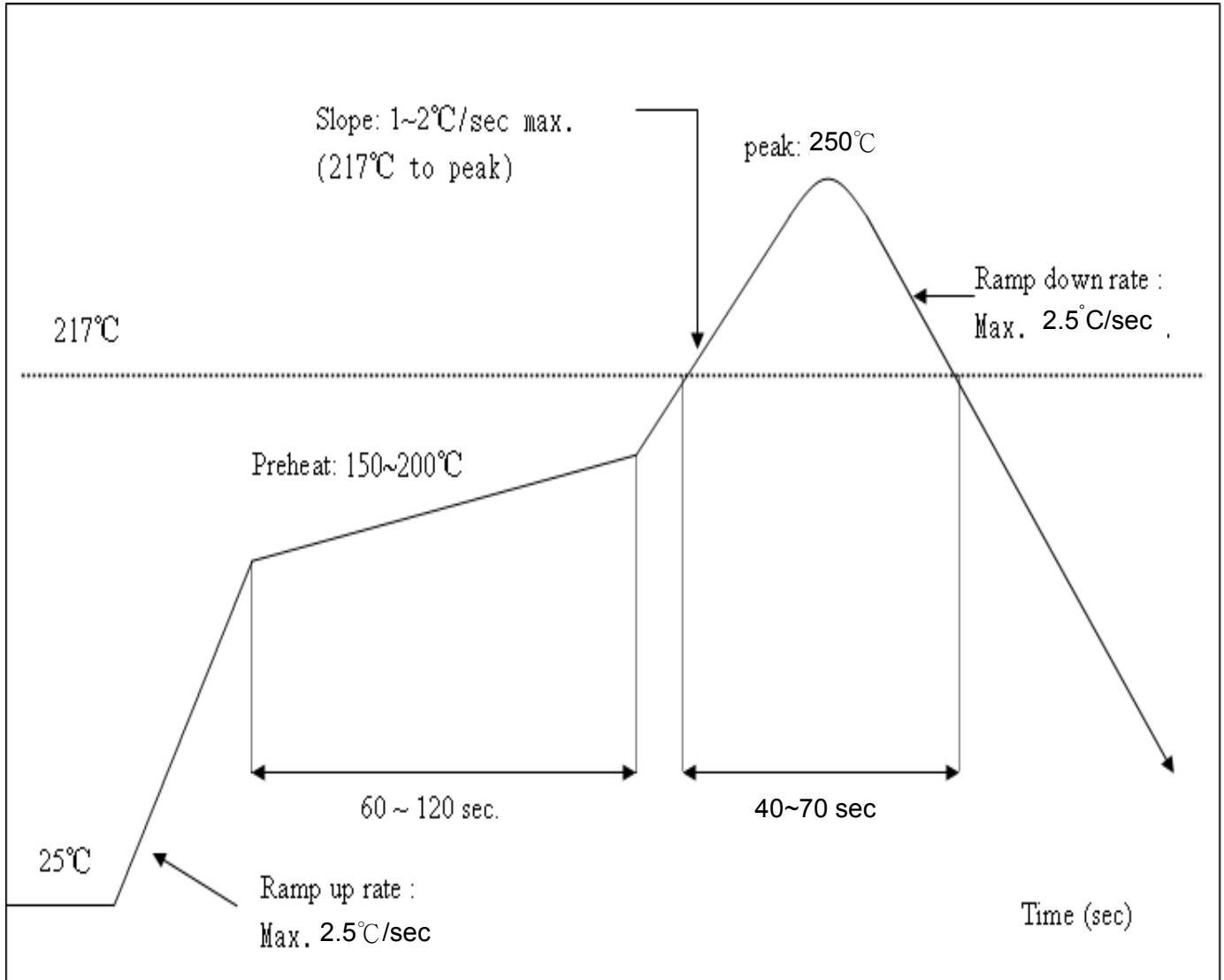
The recommend landing pad size is 0.7x1.5mm and the pin pitch is 1.2mm.



# 8. Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak Temperature : <math><250^{\circ}\text{C}</math>

Number of Times :  $\leq 2$  times



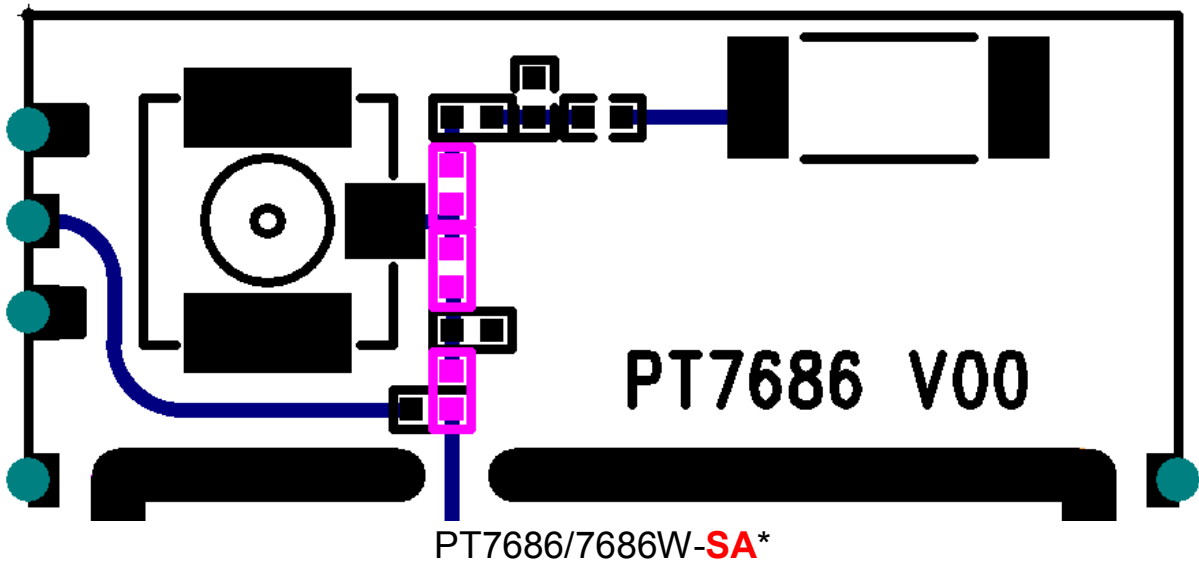


## 9. RF path and Antenna configuration

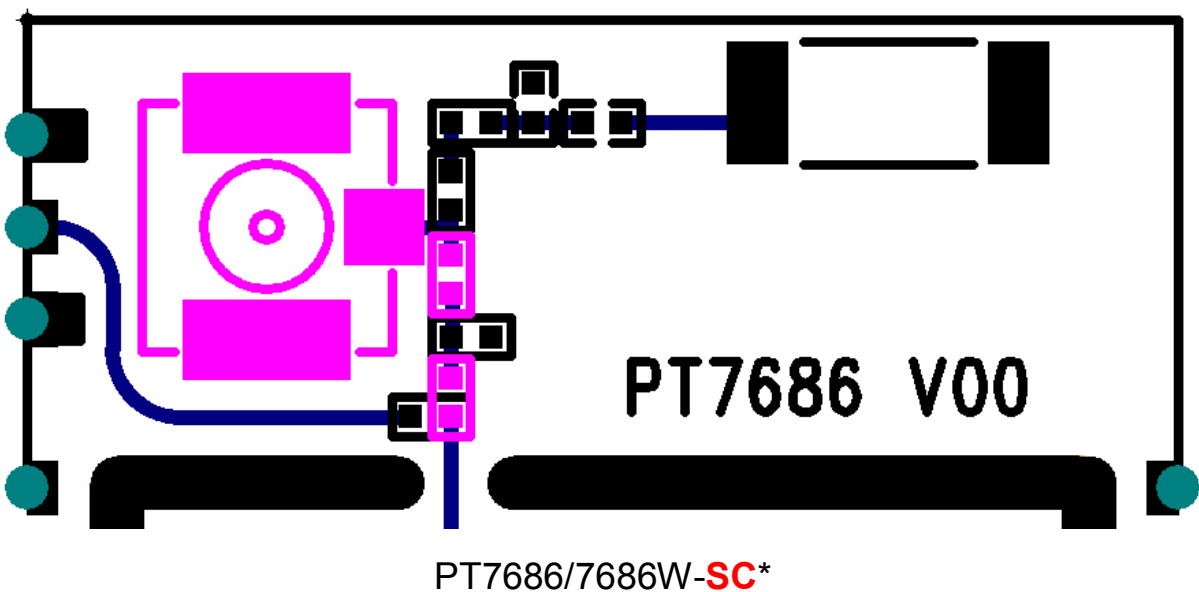
### 9.1 RF path setting

PT7686/7686W-S has four different variants of products that provide flexible of antenna selections to optimize the application.

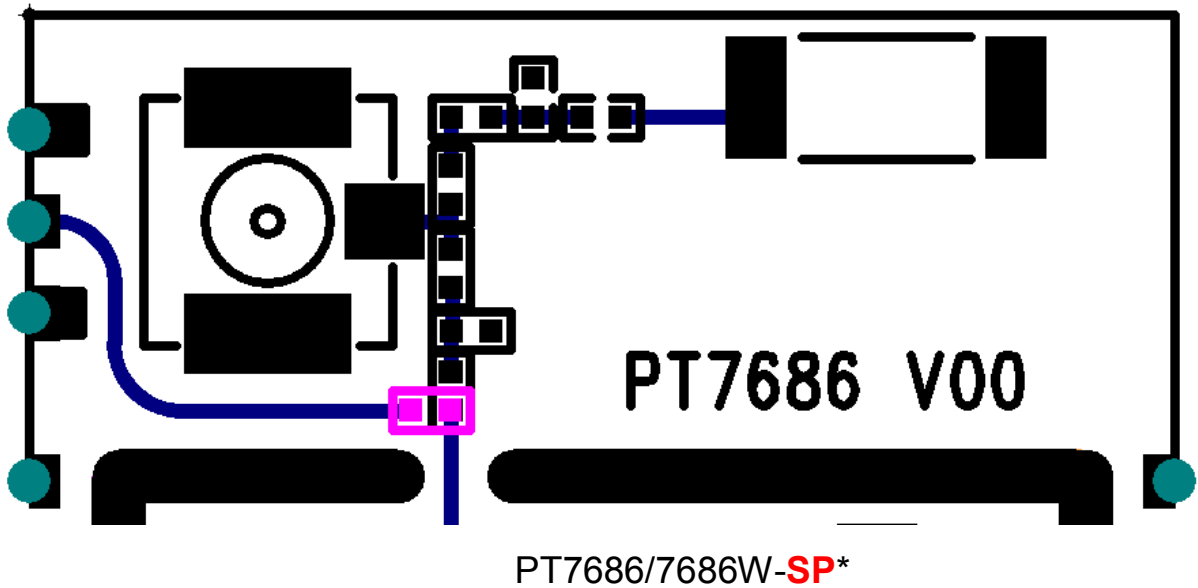
PT7686/7686W-**SA**\* using the Chip Antenna on the module. C17,C18 and C19 shown in below is mounted on the board to have RF path to the on board PCB antenna.



On PT7686/7686W-**SC**\*, C18, C19 and U.FL connector are mounted to enable customer using external cable antenna with U.FL mating connector.



PT7686/7686W-**SP**\* has C14 installed to bring RF signal to the pin-37 of the module. This allow to support antenna diversity feature. Please consult Pocom for further information support.



## 9.2 Antenna configuration

TBD